VS-VSKCS440/030

Vishay Semiconductors





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PRODUCT SUMMARY	
I _{F(AV)}	440 A
V _R	30 V

ADD-A-PAK Gen 7

Two diodes common cathode

MECHANICAL DESCRIPTION

Package

Circuit

The ADD-A-PAK Gen 7, new generation of ADD-A-PAK module, combines the excellent thermal performances obtained by the usage of exposed direct bonded copper substrate, with advanced compact simple package solution and simplified internal structure with minimized number of interfaces.

FEATURES

- 150 °C T_J operation
- Low forward voltage drop
- High frequency operation
- Low thermal resistance
- UL approved file E78996
- · Designed and qualified for industrial level
- Material categorization: for definitions of compliance please see <u>www.vishay.com/doc?99912</u>

BENEFITS

- Excellent thermal performances obtained by the usage of exposed direct bonded copper substrate
- High surge capability
- Easy mounting on heatsink

ELECTRICAL DESCRIPTION / APPLICATIONS

The VS-VSKCS440/030 Schottky rectifier common cathode has been optimized for low reverse leakage at high temperature. The proprietary barrier technology allows for reliable operation up to 150 °C junction temperature.

Typical applications are in high current switching power supplies, plating power supplies, UPS systems, converters, freewheeling diodes, welding, and reverse battery protection.

MAJOR RATINGS AND CHARACTERISTICS				
SYMBOL	CHARACTERISTICS	VALUES	UNITS	
I _{F(AV)}	Rectangular waveform	440	А	
V _{RRM}		30	V	
I _{FSM}	t _p = 5 μs sine	27 000	А	
V _F	200 A _{pk} , T _J = 125 °C	0.61	V	
TJ	Range	-55 to +150	°C	

VOLTAGE RATINGS				
PARAMETER	SYMBOL	VS-VSKCS440/030	UNITS	
Maximum DC reverse voltage	V _R	30	V	
Maximum working peak reverse voltage	V _{RWM}		V	



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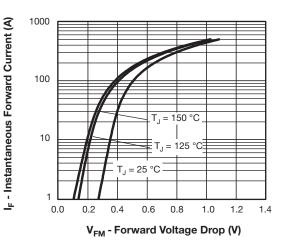
ABSOLUTE MAXIMUM RATINGS						
PARAMETER SY		SYMBOL	TEST CONDITIONS		VALUES	UNITS
Maximum average	per module		$I_{F(AV)}$ 50 % duty cycle at T_C = 97 °C, rectangular waveform		440	
forward current	per leg	IF(AV)			220	
Maximum peak one cycle		5 µs sine or 3 µs rect. pulse	Following any rated load condition and with	27 000	А	
non-repetitive surge current		IFSM	10 ms sine or 6 ms rect. pulse	rated V_{RRM} applied	3000	
Non-repetitive avalanche energ	у	E _{AS}	E _{AS} T _J = 25 °C, I _{AS} = 20 A, L = 1 mH		198	mJ
Repetitive avalanche current		I _{AR}	Current decaying linearly to zero in 1 μ s44Frequency limited by T _J maximum V _A = 1.5 x V _R typical44		А	

ELECTRICAL SPECIFICATIONS					
PARAMETER	SYMBOL	TEST CONDITIONS		VALUES	UNITS
	V _{FM}	220 A	T _J = 25 °C	0.68	V
Maximum forward voltage drop		440 A		1.0	
Maximum forward voltage drop		220 A	T _J = 125 °C	0.61	
		440 A		0.93	
Maximum reverse leakage current		T _J = 25 °C	V _R = Rated V _R	20	mA
Maximum reverse leakage current	I _{RM}	T _J = 125 °C		1120	ША
Maximum junction capacitance	CT	$V_{\rm R}$ = 5 $V_{\rm DC}$ (test signal range 100 kHz to 1 MHz), 25 °C		14 800	pF
Typical series inductance	L _S	Measured lead to lead 5 mm from package body		5.0	nH
Maximum voltage rate of change	dV/dt	Rated V _R		10 000	V/µs
Maximum RMS insulation voltage	V _{INS}	50 Hz		3000 (1 min) 3600 (1 s)	V

THERMAL - MECHANICAL SPECIFICATIONS					
PARAMETER		SYMBOL	TEST CONDITIONS	VALUES	UNITS
Maximum junction and storage temperature range	1	T _J , T _{Stg}		-55 to +150	°C
Maximum thermal resistance, junction to case per leg		R _{thJC}	DC operation	0.26	°C/W
Typical thermal resistance, case to heatsink per module		R _{thCS}		0.1	C/ W
Approximate weight				75	g
Approximate weight				2.7	oz.
Mounting torgue ± 10 %	to heatsink		A mounting compound is recommended and the torque should be rechecked after a period of 3 h to allow for the		Nm
	busbar		spread of the compound.	3	INIT
Case style			JEDEC®	TO-240AA co	ompatible

VS-VSKCS440/030

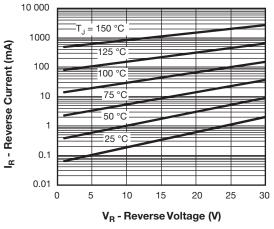
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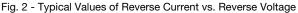


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Fig. 1 - Maximum Forward Voltage Drop Characteristics





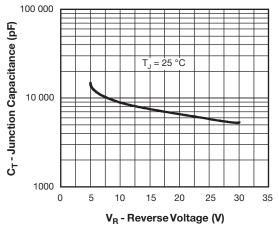
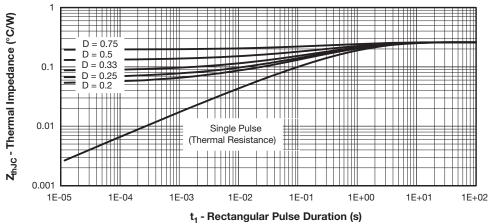


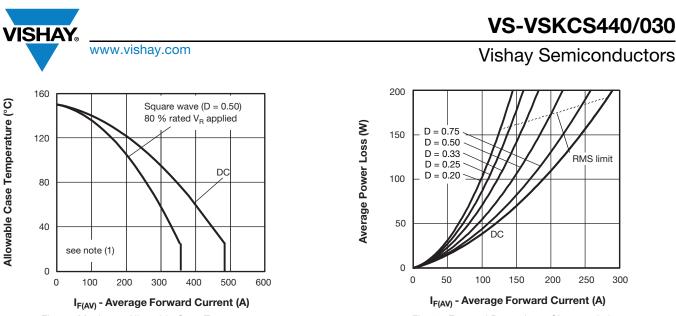
Fig. 3 - Typical Junction Capacitance vs. Reverse Voltage

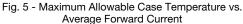


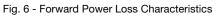


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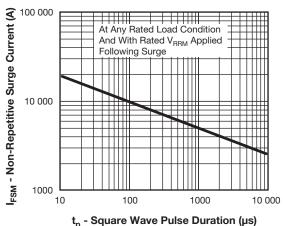


Fig. 7 - Maximum Non-Repetitive Surge Current

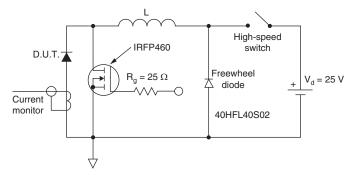


Fig. 8 - Unclamped Inductive Test Circuit

Note

- ⁽¹⁾ Formula used: $T_C = T_J (Pd + Pd_{REV}) \times R_{thJC}$;
- Pd = Forward power loss = $I_{F(AV)} \times V_{FM}$ at ($I_{F(AV)}/D$) (see fig. 6); Pd_{REV} = Inverse power loss = $V_{R1} \times I_R$ (1 - D); I_R at V_{R1} = 80 % rated V_R

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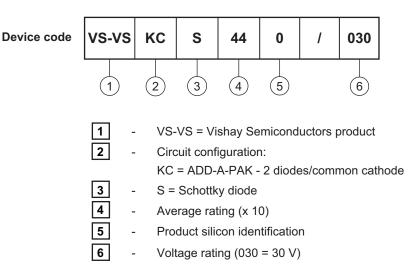
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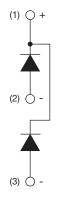
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ORDERING INFORMATION TABLE



CIRCUIT CONFIGURATION



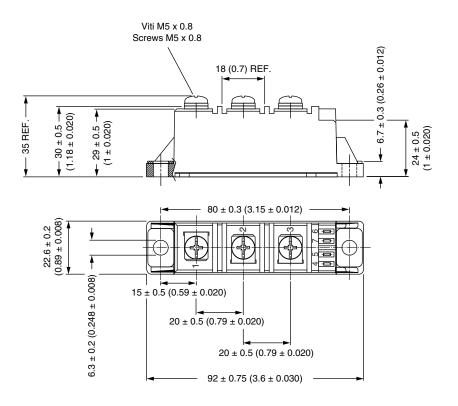
LINKS TO RELATED DOCUMENTS		
Dimensions	www.vishay.com/doc?95369	

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ADD-A-PAK Generation VII - Diode

DIMENSIONS in millimeters (inches)





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